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Analysis, Design and Control of Switching Capacitor Based Buck-Boost Converter

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***Abstract*— A switching-capacitor based buck-boost converter (with common ground) for point of load applications is proposed in this paper. It is capable of operating in stand-alone buck or boost mode in addition to its primary operation of performing the buck-boost conversion. The striking feature of the proposed converter is low source current ripple content irrespective of its mode of operation (buck-boost, buck, or boost). Firstly, feasible pulse width modulation (PWM) schemes for the proposed converter are identified and thereafter the corresponding circuit performance analysis, steady-state analysis and state-space modelling is established. Through steady-state analysis, voltage gain expressions are formulated and equations defining L-C components are derived in terms of their ripple quantities. The state-space models are used to formulate small-signal analysis and to obtain the relevant transfer functions required in the controller design. A voltage-mode/current-mode controller is designed, with a trade-off in bandwidth, to control the proposed converter and transit it from buck to boost mode or vice-versa seamlessly. A 30 ~ 55 Watt, 100 kHz, prototype point of load converter with 36 V input dc source is built to supply power at constant load voltage of either 48 or 28 V. The proposed converters' effectiveness is demonstrated experimentally in terms of reduced source current ripple along with seamless transition from buck to boost mode and vice-versa.**

***Index Terms*— Buck-boost converter, Point of load converter, State-space model, Two-switch buck-boost converter, Voltage-mode controller.**

I. Introduction

With technological advancements, the requirement of power conversion at high frequencies is soaring and is dominant in applications requiring low power for their operation. Converters for point of load applications are being developed by the designers with special emphasis laid on achieving higher conversion efficiency at full-load, increased power density, and lower radiation. Use of several point of load converters is common in low power dc system wherein many design challenges [1]-[11] must be resolved by the application engineer so as to ensure reliable power distribution. Some of these challenges are: (i) formulation of transformerless non-isolated topologies because the minimization or elimination of transformer leakage inductance is a difficult task, (ii) achieving reduced ripples with minimal L, C component requirement, and (iii) reduction in size and weight of the filtering components which results in enhanced power densities. Many dc-dc conversion circuits are present in the literature which produce stable voltages to drive the dc-loads and are briefly classified as: (i) bucking based circuits, (ii) boosting circuits, and (iii) buck-boost and other higher-order or derived converter circuits. These converters find broad application in areas pertaining to controlled power such as: (i) customized low-power integrated circuits, (ii) powering compact and tiny automotive loads, (iii) sophisticated loads such as bio-medical equipment, (iv) internet, wide and local area network services, and (v) telecommunication power supply systems, on-board spacecraft power systems, and defence equipment etc.

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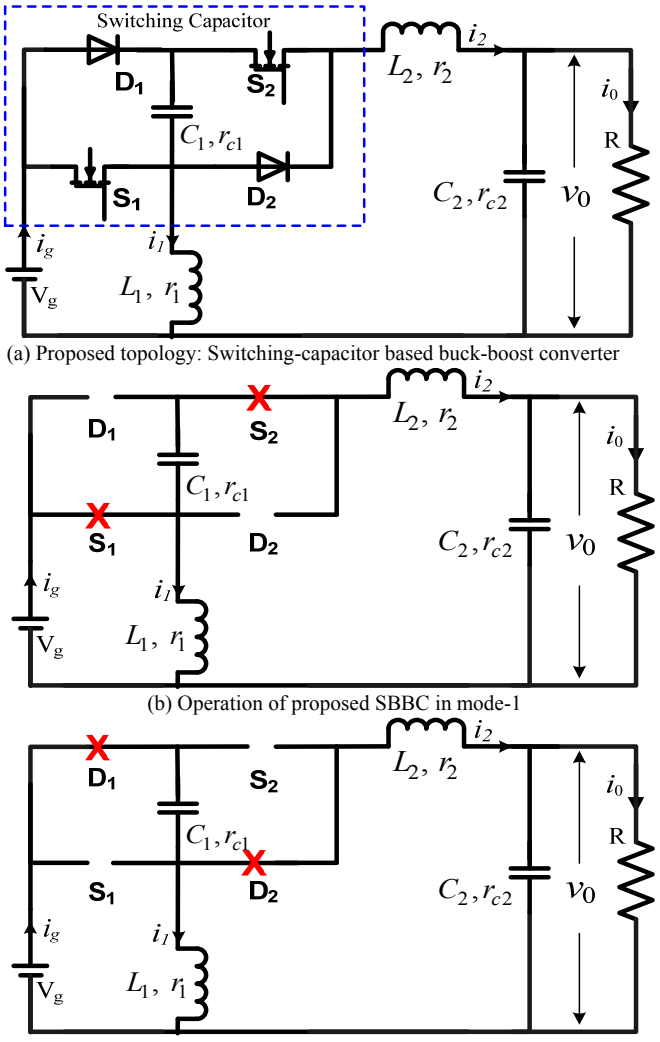

(a) Proposed topology: Switching-capacitor based buck-boost converter

(b) Operation of proposed SBBC in mode-1

(c) Operation of proposed SBBC in mode-2

Fig. 1. Proposed topology: Switching-capacitor based buck-boost converter.

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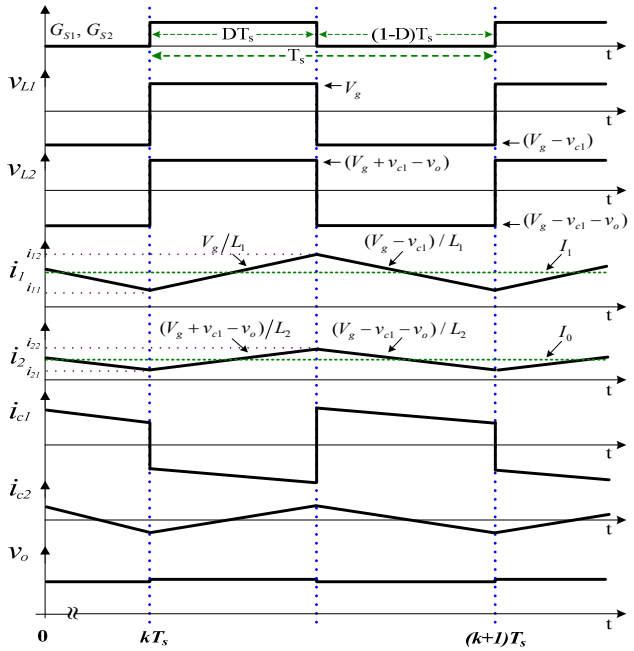

Fig. 2. Key operational waveforms of the SBBC in Type-A operation.

Recently, Fuel-cell (FC) power systems have become an attractive alternative in providing back-up power in many stand-alone applications [12]. However, they are not stiff voltage sources and thus their output voltages vary over wide ranges (e.g. 22 ~ 50 V [12]). Even in automotive vehicle applications, a similar trend in the voltage variation is seen where 12/ 24 V dc-supply systems are more popular [13] and the voltage magnitude variation is from 9 to 16 V in the 12 V bus; while it is 18 to 32 V in 24 V bus. In this scenario, the buck-boost topologies provide a viable solution to supply power to loads at constant voltage.

Conventional buck-boost converter (CBBC) is widely used to feed loads which need both voltage bucking as well as boosting [2]-[3]. It has the following salient features: (i) simplicity in structure, (ii) easy converter control due to single switch topology, and (iii) minimum number of energy storage L, C elements thus constituting a second-order system. However, high ripple content and inverted load voltage polarity are the limiting factors of CBBC which affects the input battery life and its reliability. The buck-boost converter with input filter (BBCIF) is able to reduce the source current ripple at the expense of increased system order [4]. However, addition of only the input filter is not recommended because at times it induces unwanted oscillations and may force the system into instability [4]. The insertion of a damping network in the L-C filter helps to stabilize the system by reducing the oscillations. Buck converter cascaded with boost converter (BUBS) or vice-versa i.e. boost converter cascaded with buck converter (BSBU), provides positive load voltage polarity [5]-[6]. However, the selection and design of an appropriate controller becomes essential [7] as these are fourth-order systems and an improper controller may lead to destabilization of the cascaded system.

An attempt to reduce the number of L-C elements in BUBS, from four to two, resulted in a two-switch buck boost converter (TSBBC) [8]-[9]. This topology has two controlled switches and two diodes, its structure is simple like CBBC and it also offers flexibility in its control. Several studies [10]-[11] pertaining to performance improvement of TSBBC [12]-[14] and its controlling aspects have been reported in the literature. To further enhance the degree of control flexibility, a four-switch buck-boost converter (FSBBC) [15] is evolved by replacing the two diodes with controlled switching devices. This topology offers efficiency improvement against wide variations in the dc-supply voltage but at the cost of increased gate driver requirements associated with four controlled switching devices. TSBBC with an L-C input filter (TSBBF) is reported in [16] to reduce the ripple content on the source side. To overcome some of the limitations of TSBBC, a fourth-order buck-boost converter was reported in [17] where the converter operation was explained in the boost mode. KY converters and their derivatives [18] are popular in realizing the boost based topologies. Using these structures along with additional L-C elements, a fifth-order buck-boost KY converter (FOKYC) was reported in [19]. Although this is a fifth-order topology but it has no right half of s-plane zero (RHPZ) in its control-to-output transfer function and thus it offers improved dynamic performance. Furthermore, FOKYC exhibits lower output voltage ripple due to the presence of L-C filter at the load side. However, the source current ripple is high like in CBBC. Further, it needs a half-bridge driver with a suitable dead-band like in the synchronous buck converter. A new buck-boost converter, restructured form of TSBBC, with low voltage stress has been reported [20]. Though the number of L-C elements and switching devices are identical to TSBBC, but the load ground is isolated from the source ground. Many higher order single switch buck-boost topologies have been presented in the open literature [21]-[22]. Many of these topologies provide the desired voltage gain at low/moderate duty ratios but at the expense of increased system order which in turn restricts the achievable dynamic performance. To combat the limitations prevailing in the aforementioned converters, a switching-capacitor based buck-boost converter (SBBC) is presented in this paper to address the following objectives:

(i) To achieve smooth source current waveform with low ripple content and that too by using the same number of devices as present in TSBBC;
(ii) To exhibit low source current ripple irrespective of the mode of operation unlike other converters where this feature is either absent or is present only in a few operating modes;
(iii) To exhibit minimum-phase behaviour in Type-A operation;
(iv) To obtain absolute voltage gain same as CBBC with additional feature of common ground;
(v) To accomplish transition seamlessly from buck to boost mode or vice-versa;
(vi) To achieve flexibility in the stand-alone operations involving minimal structural changes.

Steady-state analysis, state-space modelling, energy storage element component design, control aspects and performance comparison of SBBC are presented in the upcoming sections.

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II. Modelling and Analysis of Switching-Capacitor Based Buck-Boost Converter

A fourth-order switching-capacitor based buck-boost converter is evolved in this paper and shown in Fig. 1. It comprises of a bridge arm containing the active components (switches S_1, S_2 with diodes D_1, D_2) and a capacitor C_1. It is through this bridge that transfer of energy takes place from source to the load. The two controllable switches of the proposed SBBC provides the following possible control gating schemes: (i) Type-A operation: both switches S_1 and S_2 are in pulse width modulation (PWM) simultaneously, (ii) Type-B operation: S_1 is completely OFF and S_2 is in PWM mode, (iii) Type-C operation: S_1 is in PWM mode and S_2 is continuously in ON-state, (iv) S_1 is continuously in ON-state and S_2 is in PWM mode, and (v) S_1 is in PWM mode S_2 is completely in OFF-state. Amongst these schemes, the first three controlling schemes offer feasible power conversion while the subsequent two needs additional modifications in the circuit to cater reliable power conversion. With the aim to operate SBBC without reconfiguring or introducing additional circuit elements, an attempt is made in this paper to operate the converter using the first three gating control schemes only, as listed in Table–I, so that reliable power conversion is achieved.

A. Analysis of Switching Capacitor Based Buck-Boost Converter in Type-A Operation

The SBBC topology shown in Fig. 1 performs Type-A operation when its controllable switches S_1 and S_2 undergo PWM mode simultaneously. With this switching action (S_1 and S_2 in PWM together), the capacitor C_1 is connected either at the source side or load side. It is this switching action of the capacitor C_1 which is primarily responsible for the transfer of energy from source to load. When the switches (S_1, S_2) are ON (mode-1), C_1 gets connected to load side via inductor L_2, whereas with D_1, D_2 are ON together (mode-2), C_1 gets connected to the source via inductor L_1. Due to this interconnection of C_1 with input dc-source in both the modes (either through L_1 or L_2), the source current is always equal to the sum of the two inductor currents. As the inductor (L_1 and L_2) currents are continuous in nature with less ripple content, the dc-source current also exhibits limited ripple content. Although the proposed SBBC has two extra switching devices over CBBC, but it possesses the following salient features: (i) buck-boost features like that of CBBC and conventional TSBBC, (ii) lesser source current ripple for Type-A to Type-C operations, (iii) positive output voltage polarity with common ground between the source and load, and (iv) seamless mode transitions from buck to boost or vice-versa.

B. Steady-state Performance Analysis of SBBC in Type-A Operation

Time-domain analysis of SBBC is established here under the following assumptions: (i) components are ideal, (ii) resistive and energy storage components are linear time-invariant, (iii) all controlled and uncontrolled switching devices are ideal, i.e. zero voltage drop during ON-state, and (iv) switching time-period is very small compared to SBBC circuit time constant. The key waveforms shown in Fig. 2 are useful in obtaining various currents and voltages, voltage gain and design expressions of energy storage L-C elements. As discussed above, the SBBC operates in Type-A when its two switching devices (S_1, S_2) are simultaneously turned-ON/OFF while the diodes (D_1, D_2) are simultaneously operating in inverse fashion i.e. turned-OFF/ON. Due to ON-OFF operation of devices (S_1, S_2, D_1, D_2), the SBBC exhibits two different modes as shown in Fig. 1b and 1c. These equivalent circuits are used to establish KVL/KCL identities, for application of volt-sec/charge-sec balance equations for L-C elements and to finally obtain voltage buck-boost features. In the first mode, energy is stored in L_1, L_2 and C_1 while C_2 supplies energy to the load. In the second mode, stored energy is transferred to the load via C_1, L_2 together with simultaneous charging of capacitor C_2. From KVL identities, the voltage across inductive components L_1, L_2 is obtained as: (i) In mode-1: $v_{L1} = V_g$, $v_{L2} = (V_g + v_{c1} - v_o)$; (ii) In mode-2: $v_{L1} = (V_g - v_{c1})$; $v_{L2} = (V_g - v_{c1} - v_0)$. Application of volt-sec balance to the inductor L_1 gives the identity defined by eqn. 1.

$$(D)(V_g) + (1-D)(V_g - v_{c1}) = 0 \tag{1}$$

Simplifying the above equation results in $v_{c1} = V_g/(1-D)$, which means that the capacitor C_1 connected at the source side of the SBBC performs the boosting action. Similar approach is extended to the inductor L_2 resulting in eqn. 2.

$$(D)(V_g + v_{c1} - v_o) + (1-D)(V_g - v_{c1} - v_0) = 0 \tag{2}$$

Incorporating the identity obtained from eqn. 1 together with simplification of eqn. 2 results in the voltage gain expression of SBBC given by eqn. 3. This voltage gain is identical to the gain of CBBC (that too with non-inverted polarity), TSBBC and many other buck-boost converters.

$$M_{Type-A} = \left(\frac{v_0}{V_g}\right) = \frac{D}{(1-D)} \tag{3}$$

For the given input-output specifications, the energy storage elements (L_1, L_2, C_1, and C_2) need to be properly designed so as to meet various ripple standards. From the key waveforms shown in Fig. 2, the ripple currents and voltage expressions can easily be derived using simple time-domain and steady-state analysis along with the network equations. The respective currents of inductor L_1 and L_2 are**:**

$$i_1(t) = \begin{cases} \left(\frac{V_g}{L_1}\right)t + i_{11}; & \text{for } (k-1)T_s < t < (k-1)DT_s \\ \frac{(V_g - v_{c1})}{L_1}(t - DT_s) + i_{12}; & \text{for } (k-1)DT_s < t < kT_s \end{cases} \tag{4}$$

$$i_2(t) = \begin{cases} \frac{(V_g + v_{c1} - v_o)}{L_2}t + i_{21}; & \text{for } (k-1)T_s < t < (k-1)DT_s \\ \frac{(V_g - v_{c1} - v_o)}{L_1}(t - DT_s) + i_{22}; & \text{for } (k-1)DT_s < t < kT_s \end{cases} \tag{5}$$

From the above two equations, the ripple currents obtained are:

$$\Delta i_1 = DV_g/(L_1 f_s) \tag{6}$$

$$\Delta i_2 = 2DV_g/(L_2 f_s) \tag{7}$$

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TABLE -I. FEASIBLE OPERATING CASES OF THE SBBC

Operation		Type-A	Type-B	Type-C
PWM Scheme	S_1	PWM	OFF	PWM
	S_2	PWM	PWM	ON
Nature of SBBC		Buck-Boost	Buck	Boost
Voltage Gain		$D/(1-D)$	D	$1/(1-D)$
Nature of Source current		Continuous	Continuous	Continuous
Load voltage polarity		Positive	Positive	Positive

The source current expression $i_g = (i_1 + i_2)$ is valid equally for both the equivalent circuits given in Figs. 1b and 1c. Accordingly, the average source current is given by

$$I_g = (I_1 + I_2) \tag{8}$$

where I_1, I_2 are the average currents flowing through inductors L_1 and L_2 respectively. Inductor L_2 is connected at the load side and its average current is equal to the load current, i.e. $I_2 = I_0$. Assuming the power loss within SBBC to be negligible, the power balance in the converter is maintained and is mathematically represented as $V_g I_g = V_0 I_0$. Using this power balance identity along with eqn. (3), the average current drawn from source V_g is obtained as:

$$I_g = DI_0/(1-D) \tag{9}$$

Solving eqns. (8), (9) along with average inductor current expression of L_2 ($I_2 = I_0$) results in the average current in inductor L_1 and its simplified form is

$$I_1 = (2D-1)I_0/(1-D) \tag{10}$$

The peak and valley currents of the inductor L_1 and L_2 are given below which are derived from the known inductor average and ripple current expressions using eqns. (6) to (10).

$$i_{12,11} = \left[\frac{(2D-1)V_o}{R(1-D)} \pm \frac{DV_g}{(2L_1 f_s)}\right] \tag{11}$$

$$i_{22,21} = \left[\frac{V_o}{R} \pm \frac{DV_g}{(L_2 f_s)}\right] \tag{12}$$

From Figs. 1b and 1c, the source current is $i_g = (i_1 + i_2)$. Using eqns. (9) to (12), the peak and valley values of the source current obtained are:

$$i_{g(12,11)} = \left\{\frac{DI_0}{(1-D)} \pm \left(\frac{DV_g}{2f_s}\right)\left[\frac{1}{L_1} + \frac{2}{L_2}\right]\right\} \tag{13a}$$

From the above equation the average source current is given by eqn. 9 while its ripple current expression is:

$$\Delta i_g = \left(\frac{DV_g}{f_s}\right)\left[\frac{1}{L_1} + \frac{2}{L_2}\right] \tag{13b}$$

Eqn. 13b clearly indicates the source ripple current dependency on both the inductors (L_1, L_2). From the equivalent circuits shown in Fig. 1b and 1c, the SBBC source current ripple is contributed not only by L_1 but also L_2 and its relationship is deduced mathematically as given in eqn. 13. This design equation facilitates an easy means to keep the source current ripple within permissible limits. Therefore, the inductors L_1 and L_2 selection is based on the given input/output specifications and permissible source current ripple. Analytically, many combinations of L_1 and L_2 are able to keep Δi_g within permissible limits but according to Eqn. 13b the inductor L_2 ripple content has more impact on source current ripple. Hence, a higher L_2 is recommended. However, larger inductance deteriorates the dynamic response of the SBBC, and therefore to avoid any further deterioration of dynamic response, an upper limit on inductance L_2 must be enforced. Here, the better option is to choose L_2 so as to limit its ripple content not exceeding 20 ~ 40%. Once L_2 selection is finalized, L_1 needs to be suitably chosen such that source current ripples remain within the limits.

The capacitor C_1 carries current $-i_2$ during mode-1 while $(i_1 + i_2)$ flows through it in mode-2 operation. From eqns. (11) and (12), the capacitor C_1 ripple current is

$$\Delta i_{C1} = (i_{12} + 2i_{22}) = \left\{\frac{I_0}{(1-D)} + \left(\frac{DV_g}{2f_s}\right)\left[\frac{1}{L_1} + \frac{4}{L_2}\right]\right\} \tag{14}$$

From mode-1 and 2 equivalent circuits,

$$i_2 = \left(I_{2\_avg} + \Delta i_{L2}\right) = \left(I_0 + \Delta i_{C2}\right) \tag{15}$$

Eqn. (15) indicates that the average current of inductor L_2 flows through the load while its ripple current flows through the capacitor C_2. Therefore, the capacitor C_2 ripple current is

$$\Delta i_{C2} = \Delta i_{L2} = 2DV_g/(L_2 f_s) \tag{16}$$

Eqns. (14) and (16) are used to compute the ripple voltages and they are:

$$\Delta v_{C1} = \left(\Delta i_{C1} D/(C_1 f_s)\right) \tag{17}$$

$$\Delta v_{C2} = \left(\Delta i_{C2} D/(C_2 f_s)\right) \tag{18}$$

Using the ripple current and voltage expressions (6, 7, 17 and 18) established above, SBBC component design expressions are formulated and given in Table-III.

C. Small-signal models of SBBC

Fig. 1b and 1c represents the equivalent circuits of SBBC in one switching cycle. The process of energy storage and release is discussed in Section II-B. As SBBC behaviour is essentially determined by the inductor currents and capacitor voltages, the resulting network formulations must be defined in terms of currents and voltages of the energy storage elements. Through network analysis of SBBC, a set of first-order differential equations in terms of capacitor voltages and inductor currents are formulated and transformed into compact form using matrix notation as stated in eqn. 19.

$$\left.\begin{aligned}[\dot{x}] &= [A_k][x] + [B_k][u] \\ [y] &= [E_k][x] + [F_k][u]\end{aligned}\right\rangle \quad t_k < t < t_{(k+1)} \tag{19}$$

here $[A_k]$ is the system state matrix, $[B_k]$ the input matrix, $[E_k]$ the output matrix, $[x]$ the state vector, $[y]$ the output vector, and $[u]$ is the input forcing function vector. The small-signal

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transfer functions, both in s and z-domain, can easily be obtained from eqn. 19 after its linearization [23]. The state-space model matrices for Type-A Operation are:

$$[A_1]=\begin{bmatrix} \frac{-r_1}{L_1} & 0 & 0 & 0 \\ 0 & \frac{-k_{12}}{L_2} & \frac{1}{L_2} & \frac{-k_{13}}{L_2} \\ 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & \frac{k_{13}}{C_2} & 0 & \frac{-k_{13}}{RC_2} \end{bmatrix}; [A_2]=\begin{bmatrix} \frac{-k_{14}}{L_1} & \frac{-r_{c1}}{L_1} & \frac{-1}{L_1} & 0 \\ \frac{-r_{c1}}{L_2} & \frac{-k_{12}}{L_2} & \frac{-1}{L_2} & \frac{-k_{13}}{L_2} \\ \frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 \\ 0 & \frac{k_{13}}{C_2} & 0 & \frac{-k_{13}}{RC_2} \end{bmatrix}; \quad (20a)$$

$$B_1 = B_2 = [1/L_1 \quad 1/L_2 \quad 0 \quad 0]^T; [E_1]=[E_2]=[0 \quad k_{11} \quad 0 \quad k_{13}]; \quad (20b)$$

$$k_{11} = Rr_{c2}/(R + r_{c2}); k_{12} = (r_2 + r_{c1} + k_{11}); k_{13} = (k_{11}/R); k_{14} = (r_1 + r_{c1});$$

These state-space model matrices are used to generate the transfer functions and the relevant discussion is given in Section III.

D. Analysis of SBBC in Type-B and Type-C Operation

Detailed analysis of Type-A operation was explained in the above section. Following the same methodology, analysis of Type-B and Type-C operation is established and briefly explained here. In Type-B operation of SBBC, S_1 is completely OFF and S_2 is in PWM mode, while in Type-C operation the switch S_1 is in PWM mode and S_2 is continuously in the ON-state. Therefore, the SBBC equivalent circuits in Type-B or Type-C operation will also be different. In each of these operations, SBBC exhibits two different equivalent circuits and the corresponding inductor voltage expressions are tabulated in Table IV for ready use. The application of volt-sec balance to these inductor voltages followed by their simplification results in the corresponding voltage gains as listed in the same table. The state-space model matrices for Type-B and Type-C operations are also given by eqns. (21) and (22).

State-space model matrices for Type-B operation:

$$[A_1]=\begin{bmatrix} \frac{-k_{14}}{L_1} & 0 & \frac{-1}{L_1} & 0 \\ 0 & \frac{-k_{15}}{L_2} & 0 & \frac{-k_{13}}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{k_{13}}{C_2} & 0 & \frac{-k_{13}}{RC_2} \end{bmatrix}; [A_2]=\begin{bmatrix} \frac{-k_{14}}{L_1} & \frac{-r_{c1}}{L_1} & \frac{-1}{L_1} & 0 \\ \frac{-r_{c1}}{L_2} & \frac{-k_{12}}{L_2} & \frac{-1}{L_2} & \frac{-k_{13}}{L_2} \\ \frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 \\ 0 & \frac{k_{13}}{C_2} & 0 & \frac{-k_{13}}{RC_2} \end{bmatrix}; \quad (21a)$$

$$[B_1]=[B_2]=[1/L_1 \quad 1/L_2 \quad 0 \quad 0]^T; [E_1]=[E_2]=[0 \quad k_{11} \quad 0 \quad k_{13}]; \quad (21b)$$

State-space model matrices for Type-C operation:

$$[A_1]=\begin{bmatrix} \frac{-r_1}{L_1} & 0 & 0 & 0 \\ 0 & \frac{-k_{12}}{L_2} & \frac{1}{L_2} & \frac{-k_{13}}{L_2} \\ 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & \frac{k_{13}}{C_2} & 0 & \frac{-k_{13}}{RC_2} \end{bmatrix}; [A_2]=\begin{bmatrix} \frac{-k_{14}}{L_1} & 0 & \frac{-1}{L_1} & 0 \\ 0 & \frac{-k_{15}}{L_2} & 0 & \frac{-k_{13}}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ 0 & \frac{k_{13}}{C_2} & 0 & \frac{-k_{13}}{RC_2} \end{bmatrix}; \quad (22a)$$

$$[B_1]=[B_2]=[1/L_1 \quad 1/L_2 \quad 0 \quad 0]^T; [E_1]=[E_2]=[0 \quad k_{11} \quad 0 \quad k_{13}]; \quad (22b)$$

E. Performance Comparison of SBBC with other Buck-Boost Topologies

Here, SBBC performance is compared with other buck-boost converter topologies. In the proposed SBBC the two inductors L_1 and L_2 contribute towards the source current ($i_{g\_SBBC}=i_{L1}+i_{L2}$) while in conventional CUK converter [2], the source current is contributed by only inductance L_1 ($i_{g\_CUK}=i_{L1}$). With identical inductances and input/output voltages, the source current ripple is somewhat higher in the SBBC. However in SBBC and CUK converters, the ripple current in the load side capacitor C_2 is more or less same and is low on account of the second inductance L_2. Though the CUK converter exhibits little lower source ripple content over SBBC but it has many other limitations highlighted in Table II-A. Moreover, it is not feasible for multi-mode operation. For the identical input inductance L_1, input and output voltages, SBBC standalone operation in boost mode (Type-C operation) is compared with the conventional boost converter operation. The source current ripple in SBBC under Type-C operation is slightly higher over the conventional boost converter due to ripple current of inductance L_2 but the presence of inductance L_2 in SBBC and its operation in boost mode (Type-C mode) has a positive impact in terms of substantial reduction in the load side capacitor C_2 ripple current. In the conventional boost converter there is no second inductance L_2 and thus the pulsating diode ripple current flows through the load side capacitor. Therefore, SBBC operation in boost mode (Type-C operation) results in reduced capacitor stress over the conventional boost converter. After extensive analysis of various topologies listed in references, a comparison of SBBC performance parameters with other buck-boost topologies is listed in Table-II.

Figs. 1b and 1c indicate the energy transfer phenomena in the proposed SBBC wherein the dc source remains connected to load via L/C elements in both the operating modes. While in most of the buck-boost topologies, (CBBC, CUK, SEPIC etc.,), the source may not have a connection through L/C elements to the load in any of the operating modes. In many of these topologies, the energy is first stored in the L/C elements and later it is transferred to load and thus there is a finite time-delay in energy transfer from source to load. For example, in CUK converter [2], when the switch turns-ON, the energy is first stored in the inductance L_1 and is then transferred to capacitor C_1 in the subsequent switch turn-OFF duration. Thus, the load receives power from source through an indirect energy transfer and this delay impact is reflected through a right half of s-plane zero(s) (RHPZ) in the control-to-output transfer function (COTF). But in SBBC, direct energy transfer takes place from source to load on continuous basis irrespective of the switching operations, indicated in the equivalent circuits Figs. 1b and 1c, and this hidden fact can easily be understood by examining the COTF given in Section III. From multi-mode perspective all the topologies listed in Table II-B (TSBB, TSBBF, BUBS and SBBC) uses identical number of devices. But from the smooth current waveforms

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point of view, SBBC is better option than other topologies. Furthermore, SBBC belongs to a class of minimum-phase systems as its COTF has no RHP zeros and hence exhibits better dynamic performance.

F. SBBC L-C Component Design

The expressions given in eqns. 6 and 7 clearly indicate that the ripple content of L_1/L_2 is directly proportional to duty ratio. Current ripple is higher in boosting operation and thus higher inductances L_1/L_2 are needed to meet the specified ripple content. However, high inductance leads to inferior dynamic performance and thus it is difficult to meet transient performance specifications. In this paper, considering the buck operation as the basis, the design is initiated ($\Delta i_{L1} \leq 50\%$, $\Delta i_{L2} \leq 30\%$, $\Delta v_C \leq 5\%$) and the trade-off values are arrived at after enforcing the source current ripples (Δi_g=1.0 A). Using eqns. 6 to 13 with V_g=36 V and f_s=100 kHz, the inductances are computed as: (a) bucking case: V_o=28 V, R=15 Ω, D=0.44, Δi_{L1}=0.2 A, $L_1 \geq$ 792 µH, Δi_{L2}=0.374 A, $L_2 \geq$ 847 µH, Δi_g=0.6 A; (b) boosting case: V_o=48 V, R=70 Ω, D=0.6, Δi_{L1}=0.18 A, $L_1 \geq$ 1200 µH, Δi_{L2}=0.14 A, $L_2 \geq$ 3100 µH, Δi_g=0.32 A. The boosting case design ($L_1 \geq$ 1200 µH, $L_2 \geq$ 3100 µH) yields low ripples but the corresponding inductances are on higher side. A trade-off design is obtained after making a compromise in Δi_g (<1.0 A) and the final chosen inductances are: L_1=800 µH, L_2=1000 µH. Using these inductance values, ripple voltage constraint along with eqns. 17 and 18 the capacitances C_1 and C_2 are computed.

TABLE -III. SBBC PARAMETER DESIGN EXPRESSIONS

Parameter	Expression
$L_1 \geq$	$DV_g/(f_s\Delta i_1)$
$L_2 \geq$	$2DV_g/(f_s\Delta i_2)$
$C_1 \geq$	$\Delta i_{C1}D/(f_s\Delta v_{C1})$
$C_2 \geq$	$\Delta i_{C2}D/(f_s\Delta v_{C2})$

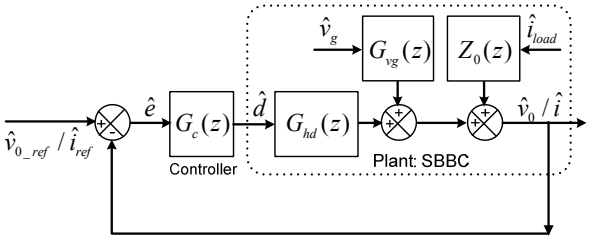
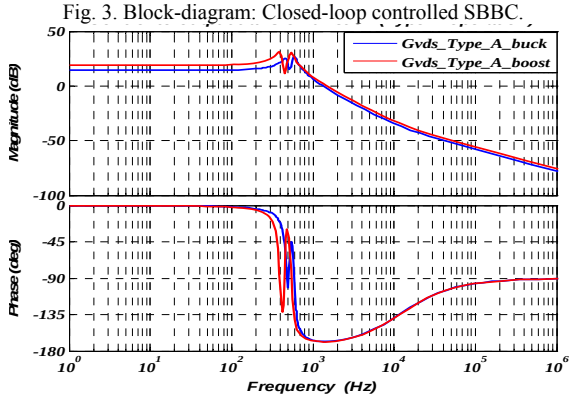
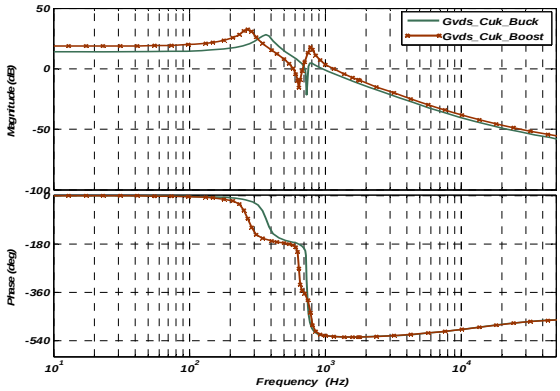


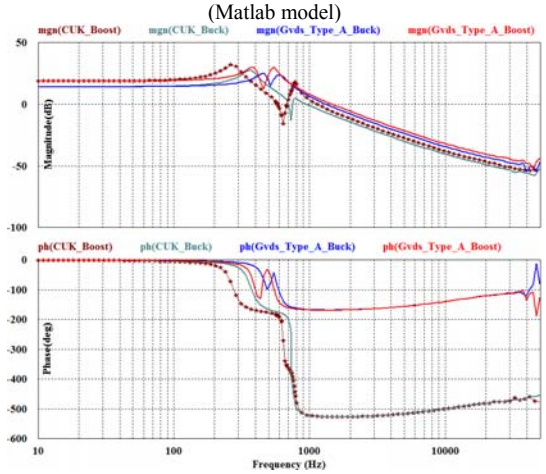
Fig. 3. Block-diagram: Closed-loop controlled SBBC.



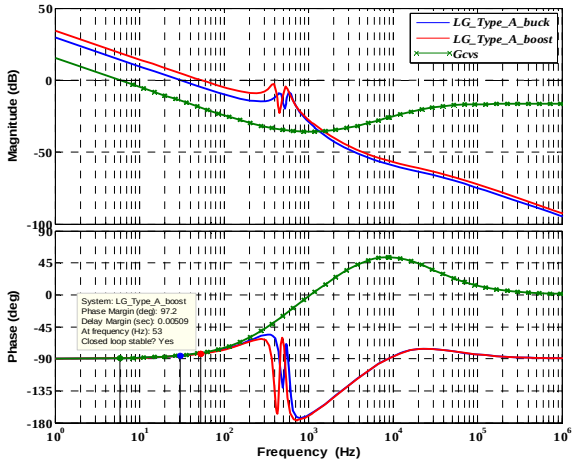
(a) Frequency response of control-to-output transfer functions (Matlab model)



(b) Frequency response of CUK converter control-to-output transfer functions (Matlab model)



(c) Frequency response of control-to-output transfer functions (SBBC and CUK, generated from PSIM simulator [26] for model verification)



(d) Loopgain frequency response plot of SBBC

Fig. 4. Frequency response plots.

TABLE -IV. INDUCTOR VOLTAGES: TYPE-B/TYPE-C OPERATION

Quantity	Type-B Operation		Type-C Operation	
	Mode-1	Mode-2	Mode-1	Mode-2
v_{L1}	$(V_g - v_{c1})$	$(V_g - v_{c1})$	V_g	$(V_g - v_{c1})$
v_{L2}	$(V_g - v_0)$	$(V_g - v_{c1} - v_o)$	$(V_g + v_{c1} - v_o)$	$(V_g - v_o)$
Voltage gain (M)	$M_{Type-B} = D$		$M_{Type-C} = 1/(1-D)$	

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III. Closed-loop Controller Design

The linear control system theory is well established and is applied in many real-time control system designs [24]. It adopts the frequency domain models for controller design and to characterize both the absolute and relative stability aspects of closed-loop controlled system. The block-diagram representation of SBBC along with single-loop voltage-mode/current-mode controller is shown in Fig. 3. Here, the plant transfer functions are: $G_{hd}(z)$, $G_{vg}(z)$, $Z_0(z)$, and they are dependent on type of operation of SBBC (Type-A, Type-B and Type-C). From the known state-space model (eqn. 19) matrices, formulated for Type-A, Type-B and Type-C operations in Section II, these plant transfer functions can easily be obtained [20]. Here, the controller transfer function $G_c(z)$ is in the feed-forward path along with the control-to-output transfer function $G_{hd}(z)$ (where $G_{hd}(z)$ is $G_{vd}(z)$ for voltage control and $G_{id}(z)$ for current control). As it is inferred that the SBBC plant transfer functions are dependent on the type of operation (Type-A, Type-B and Type-C), it is difficult to stabilize the converter using solely one unique controller. Even if the unique controller $G_c(z)$ is able to stabilize Type-A, Type-B and Type-C operation of SBBC, the achievable relative stability limits are going to be different and thus will lead to differences in the disturbance rejection capability. Furthermore, Type-C operation/boost mode presents non-minimum phase (NMP) [24] behaviour and thus the corresponding $G_c(z)$ has to have a low bandwidth. On the other hand, the Type-B operation/buck-mode yields minimum phase [24] behaviour and thus the corresponding controller $G_c(z)$ can have higher bandwidths leading to better dynamic response of the closed-loop system.

The above discussion envisages that change of SBBC operation, from Type-B to Type-C or vice-versa, must be accompanied by respective change in its controller (high to low bandwidth or vice-versa). In Type-A PWM gating scheme, the direct duty ratio control is a straight forward technique to change the SBBC operation from buck to boost or vice versa without involvement of any controller changeover mechanism. A single controller with a trade-off in bandwidth is sufficient enough to perform voltage/current regulation. In view of this, a single-loop digital voltage-mode/current-mode controller is designed in the paper using the approach mentioned in [23] to achieve the desired load voltage/current regulation. For the controller design, single-input single output tool of Matlab [25] is used and poles and zeros are placed at the desired locations such that the resulting closed-loop system exhibits absolute stability. Once it satisfies the absolute stability criterion, it becomes necessary to choose a controller which ensures the relative stability specifications. To ensure that the closed-loop SBBC performs load voltage/current regulation both in the buck and boost mode against perturbations either in the line or load side, the cross-over frequency is kept at lower side so that the loopgain frequency response has an adequate gain margin (GM) (> 6 dB or higher).

The controller design is initiated using the following SBBC parameters: L_1=800 μH, L_2=1000 μH, C_1=47 μF, C_2=100 μF. Using eqns. 19 to 22, the plant transfer functions indicated in Fig. 3 are computed. The control-to-output voltage and control-to-inductor current transfer functions for D=0.44, D=0.57 are given in eqns. 23 and 24.

$$G_{vd}(s)=\frac{[a_{4v}s^4+a_{3v}s^3+a_{2v}s^2+a_{1v}s+a_{0v}]}{[b_{4v}s^4+b_{3v}s^3+b_{2v}s^2+b_{1v}s+b_{0v}]} \tag{23}$$

$$G_{id}(s)=\frac{[a_{4i}s^4+a_{3i}s^3+a_{2i}s^2+a_{1i}s+a_{0i}]}{[b_{4i}s^4+b_{3i}s^3+b_{2i}s^2+b_{1i}s+b_{0i}]} \tag{24}$$

where the constant coefficients are: (i) D=0.44: a_{4v}=0, a_{3v}=782.2, a_{2v}=5.812xe^7, a_{1v}=2.155xe^{10}, a_{0v}=6.168xe^{14}, b_{4v}=1, b_{3v}=881.7, b_{2v}=2.264Xe^7, b_{1v}=9.946xe^9, b_{0v}=1.202xe^{14}, a_{4i}=0, a_{3i}=1.279xe^5, a_{2i}=6.105xe^7, a_{1i}=1.369xe^{12}, a_{0i}=3.393xe^{14}, b_{4i}=1, b_{3i}=881.7, b_{2i}=2.264Xe^7, b_{1i}=9.946xe^9, b_{0i}=1.202xe^{14}, (ii) D=0.57: a_{4v}=0, a_{3v}=1027, a_{2v}=7.63xe^7, a_{1v}=*1.894*xe^{10}, a_{0v}=*6.162*xe^{14}, b_{4v}=1, b_{3v}=753.7, b_{2v}=*1.771*xe^7, b_{1v}=*6.38*xe^9, b_{0v}=*6.975*xe^{13}, a_{4i}=0, a_{3i}=1.677xe^5, a_{2i}=4.732xe^7, a_{1i}=1.362xe^{12}, a_{0i}=1.937xe^{14}, b_{4i}=1, b_{3i}=753.7, b_{2i}=1.771xe^7, b_{1i}=6.38xe^9, b_{0i}=6.975xe^{13}. The controller transfer function in discrete-time domain is

$$G_{cv}(z)=\frac{k_{1v}(z+a_{1v})(z+a_{2v})}{(z+b_{1v})(z+b_{2v})} \tag{25a}$$

$$G_{ci}(z)=\frac{k_{1i}(z+a_{1i})(z+a_{2i})}{(z+b_{1i})(z+b_{2i})} \tag{25b}$$

where k_{1v}=0.15, a_{1v}=-0.9614, a_{2v}=-0.949, b_{1v}=-1.0, b_{2v}=-0.1984, k_{1i}=0.38095, a_{1i}=-0.9806, a_{2i}=-0.9849, b_{1i}=-1.0, b_{2i}=-0.5019 parameters will keep the voltage/current control loop stable. For identical parameters, the frequency response of COTF of SBBC and CUK converters is plotted in Fig. 4a to 4c. In case of SBBC, the COTF has four left half of s-plane (LHP) poles (two complex conjugate pairs) and three LHP zeros (one real and one complex conjugate pair). While the CUK converter COTF has four LHP poles (two complex conjugate pairs) and three zeros (one real LHP zero and one complex conjugate RHP zero pair). The magnitude plot trend of SBBC and CUK converters is almost similar whereas a considerable deviation is seen in the CUK converter phase plot. In SBBC, the phase starts from 0^o and rolls-off close to 180^o at the resonating frequency and due to LHP zeros it finally settles to 90^o in the high frequency region. On the other-hand, CUK converter phase start from 0^o and with increase in frequency it rolls down close to 540^o due to RHP zeros and then finally settles at 450^o. These frequency responses generated in MATLAB using the mathematical models, eqns. 19 to 22, are now validated through frequency responses obtained from PSIM circuit-simulator [26] as shown in Fig. 4c. It is seen that the model based frequency responses are in close agreement with the frequency responses obtained from the PSIM simulator. Frequency response plots of loopgain transfer functions (SBBC buck and boost operations) is given in Fig. 4d. These frequency responses clearly show the stability of the closed-loop controlled system of SBBC both in bucking and boosting mode.

IV. Experimental Results

The validity of the analytical findings of the proposed buck-boost converter established in the preceding sections is now demonstrated through experimental measurements [27]. For experimentation, a 30 ~ 55 W, 100 kHz prototype

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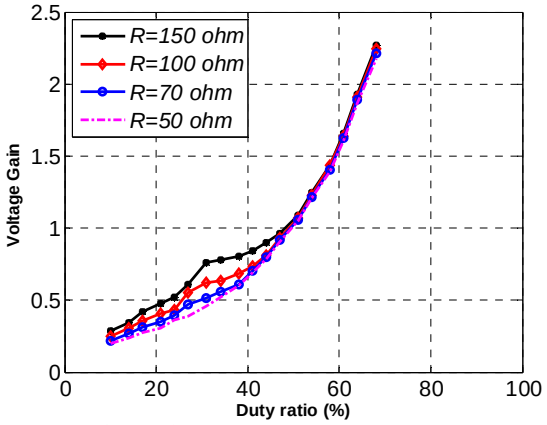
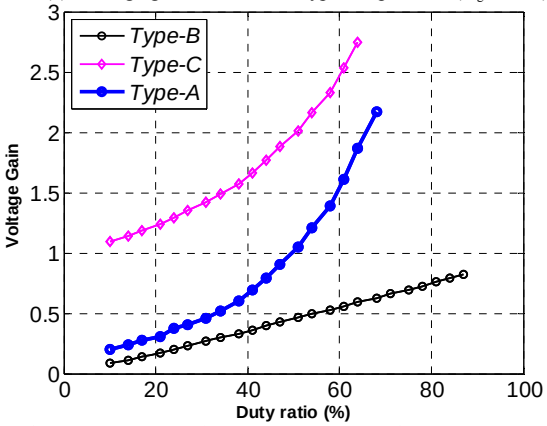
converter circuit was built using the L-C components and they are: L_1= 800 µH, L_2=1000 µH, C_1=33 µF, C_2=100 µF. A nominal voltage of 36 V is used as a dc source. The SBBC's performance both in bucking as well as in boosting mode is verified by fixing the reference load voltage to 28 V (~20% below the nominal V_g, P_o: ~53 W) in bucking mode and 48 V (~20% above the nominal V_g, P_o: 34 W) in boosting mode. Keeping the nominal source voltage as 36 V, the voltage gain of the SBBC is measured by varying the duty-ratio and is plotted in Fig. 5a for different loads (R=150, 100, 70 and 50 Ω). It is seen that the voltage gain increases with increase in the duty-ratio. Further, for duty-ratios less than 50%, the voltage gain remains less than one which implies bucking action of SBBC in Type-A operation. However, a slight variation in the gain of SBBC is observed at different loads, which is due to the loading effect. At higher loads (R=50 Ω) the parasitic voltage drops are dominant, like in other dc-dc converter systems, leading to a slight fall in the voltage gain.

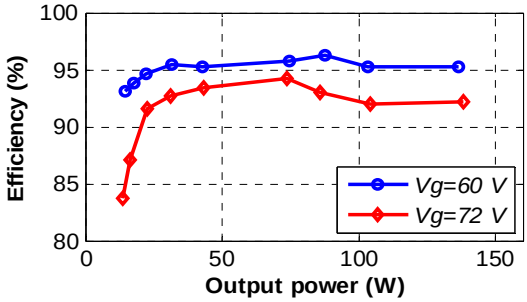


(a) Voltage gain of SBBC in Type-A operation (V_g: 36 V)

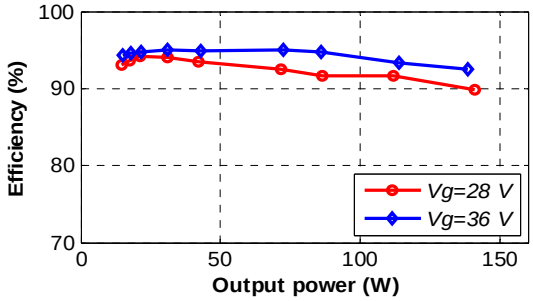


(b) Voltage gain of SBBC in Type-A, Type-B and Type-C (V_g: 36 V)

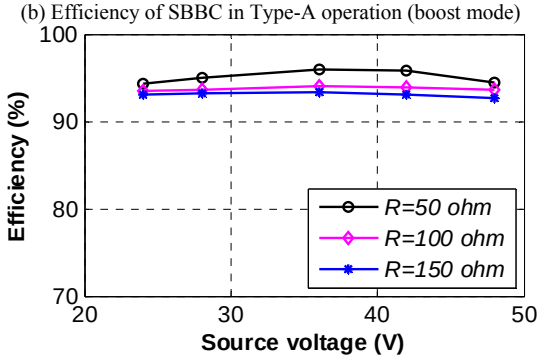
Fig. 5. Measured voltage gain variation with duty ratio.



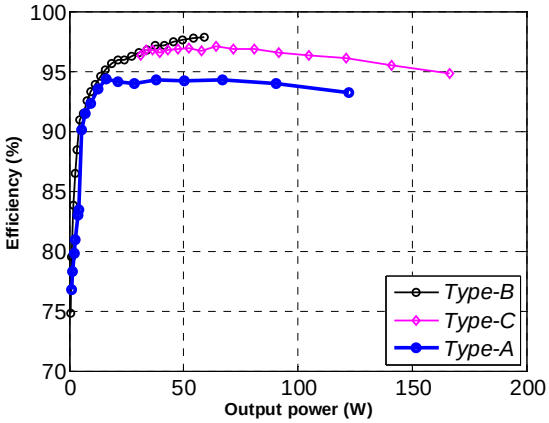
(a) Efficiency of SBBC in Type-A operation (buck mode)



(b) Efficiency of SBBC in Type-A operation (boost mode)



(c) SBBC efficiency variation with input supply voltage (Type-A operation)



(d) Efficiency of SBBC in Type-A, Type-B and Type-C operations

Fig. 6. Measured SBBC efficiency variation with power output and supply voltage.

The SBBC mode changeover from buck to boost takes place close to 50% of duty ratio for all the loads as seen in Fig. 5a. For the duty ratios above 50%, the gain of SBBC is rising indicating its boosting behavior. A similar trend is seen for all loading conditions mentioned above but the impact of the loading on the voltage gain is negligible, unlike in the bucking mode. Further, the SBBC voltage gain is also measured for the Type-B and C operations and is compared with the Type-A operation as shown in Fig. 5b. The measured voltage gain plots obtained closely resemble the conventional buck and boosting operations. This substantiates the flexibility of SBBC, which supports all three operations (buck-boost, buck and boost) without the use of additional circuit elements and exhibits seamless transitions. The variation of efficiency with power output for all the three operating modes is shown in Fig. 6. Here, the efficiency of SBBC in Type-A operation is measured for two different cases, which are: (a) Fig. 6a- Buck mode: V_g=60, 72 V, V_o=48 V, (b) Fig. 6b- Boost mode: V_g=28, 36 V, V_o=48 V. In both these test conditions, the

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SBBC exhibited efficiency close to 95%. However, a slight fall in efficiency is observed in the cases ((V_g=72 V, V_o=48 V), (V_g=28 V, V_o=48 V)) where SBBC involves more bucking/boosting. The efficiency plot for variation in the input voltage is shown in Fig. 6c. It is seen that the SBBC exhibits higher efficiencies at higher loading conditions and it is slightly less efficient at lighter loads. The fall in the efficiency in the latter case is because of more losses. The SBBC efficiency variation with power output for Type-A, B and C operation is shown in Fig. 6d. Here, Type-B/Type-C operations exhibit a little higher efficiency compared to Type-A operation because the former case uses only three switching devices whereas the latter uses all the four devices together.

A controller (eqn. 25a) is designed to regulate the SBBC load voltage and to ensure closed-loop system stability against line and load variations. To begin with, SBBC load voltage reference is set to 28 V with a 70 Ω load and the start-up performance under closed-loop control is measured and is shown in Fig. 7. The steady-state waveforms of SBBC in the bucking case with V_{o_ref}=28 V are shown in Fig. 8. As seen in the figure, the inductor L_1 and L_2 currents are continuous while the source current is smooth and has low ripple content (Δi_g ~ 0.5 A). After performing rigorous characterization of SBBC under dynamic conditions, a few measurement results with illustrations are presented in Figs. 9 to 13. Firstly, the dynamic performance of SBBC in the bucking mode is given for the following test conditions: (a) load voltage regulation against change in (R) load from 70 to 25 Ω (V_g: 36 V), and (b) load voltage regulation against variation in source (V_g) from 30 to 36 V (R: 70 Ω). These dynamic tests (Fig. 9) indicate that the load voltage regulation is achieved in 7.5 ms against load variations while it takes a little longer to achieve regulated output voltage (~15 ms) against source voltage variation. Faster dynamic response of SBBC is seen in case of load variation compared to source variation. Next, to see the effectiveness of SBBC during mode transition, reference voltage is changed from 28 to 48 V and the corresponding dynamic performance measurement is shown in Fig. 10. As seen, the transition is seamless for load voltage change from 28 to 48 V and vice-versa. Furthermore, the time taken to make this transition is close to 5.0 ms. The steady-state performance of SBBC measured in boost mode is shown in Fig. 11. In this mode also the source current is smooth with low ripple content. The dynamic performance of SBBC in boost mode (Fig. 12) is alike buck mode with the following operating conditions: (a) load voltage regulation against change in (R) load from 70 to 40 Ω (V_g: 36 V), and (b) load voltage regulation against variation in source (V_g) from 30 to 36 V (R: 70 Ω). In the first case, the load voltage regulation is achieved within 3.0 ms while it takes close to 10.0 ms under source perturbations.

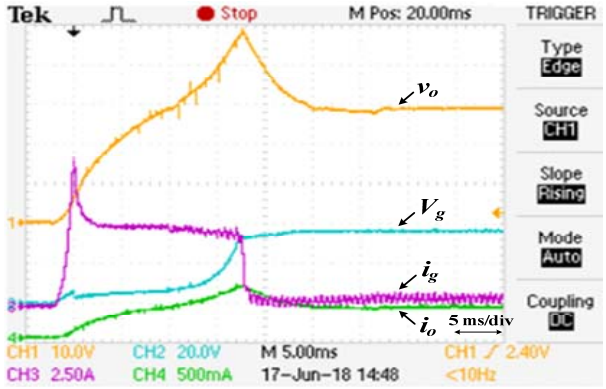
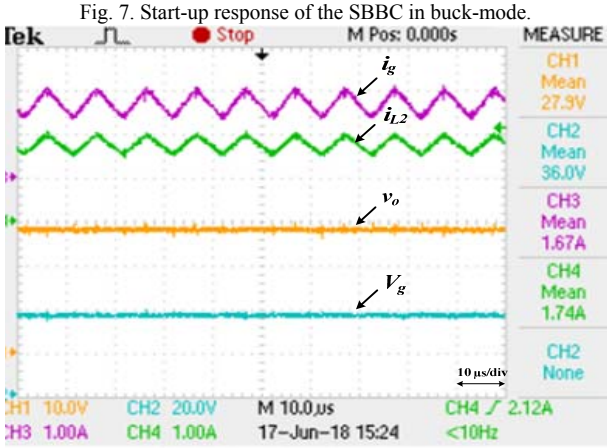
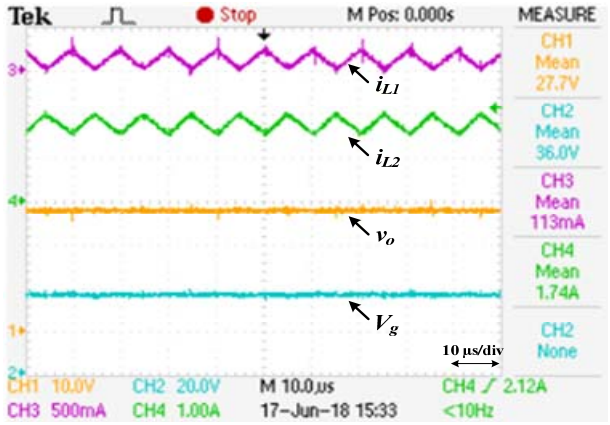


Fig. 7. Start-up response of the SBBC in buck-mode.

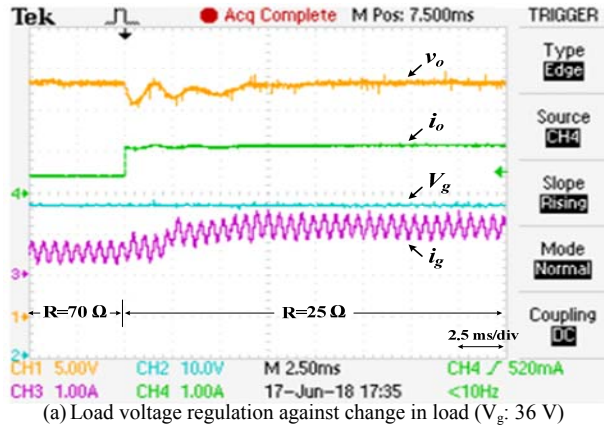


(a) Source and inductor L_2 current waveforms



(b) Load voltage and inductor L_1, L_2 current waveforms

Fig. 8. Steady-state waveforms of the SBBC under buck mode of operation (V_g: 36 V).



(a) Load voltage regulation against change in load (V_g: 36 V)

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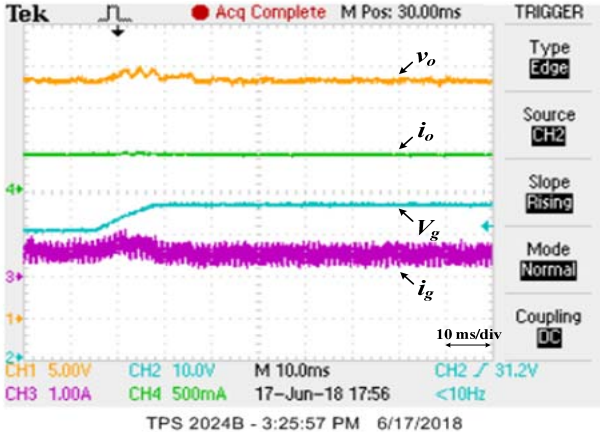
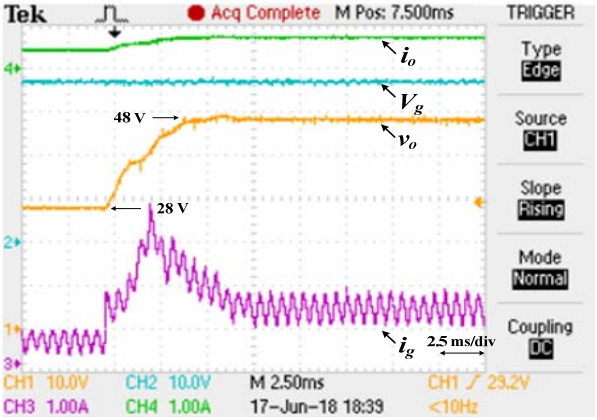
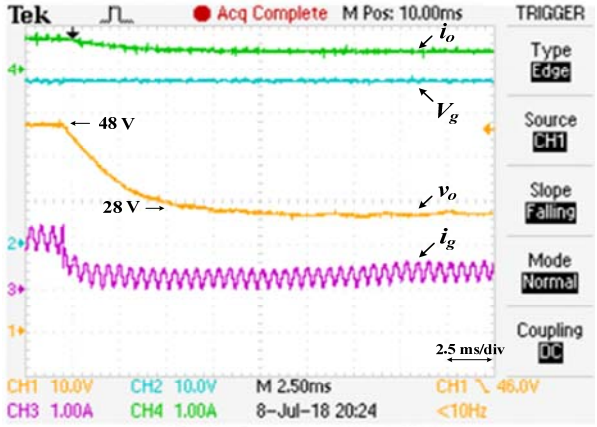


(b) Load voltage regulation against change in source voltage (V_g: 30 to 36 V, R=70 Ω)

Fig. 9. Dynamic performance of SBBC against line and load variations (buck mode of operation).



(a) Buck to boost mode of operation



(b) Boost to buck mode of operation

Fig. 10. Dynamic performance of SBBC under mode-transition (V_g: 36 V, R: 70 Ω).

The proposed SBBC's performance is also demonstrated at even higher voltage and power levels. The measured result shown in Fig. 14 (for V_g: 48 V, R: 100 Ω, V_{o_ref}: 28 to 100 V) shows its performance both in bucking as well as boosting mode. The proposed SBBC performs not only voltage regulation but also current regulation effectively. To demonstrate this, a digital current-mode controller, eqn. 25b, is designed to regulate the load current. The current-loop is designed to regulate a current of 1.0 A at a nominal source voltage of 36 V as shown in Fig. 13a and 13b. The effectiveness of current regulation is shown in Fig. 13 for variation in (i) supply voltage (28 to 42 V), (ii) load (25 to 50 Ω) and (iii) reference current (1.0 to 1.5 A). In all these cases current regulation is achieved effectively. This exhaustive experimental study reveals that SBBC is (i) maintaining low ripple content in the source current irrespective of its operating modes, (ii) successful in achieving load voltage/current regulation against line and load variations, and (iii) undergoing seamless mode transition.

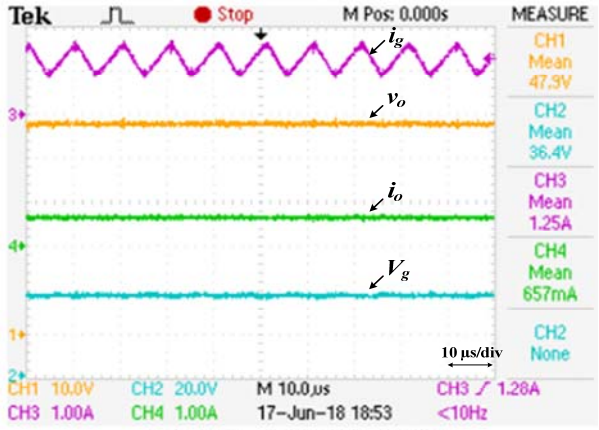
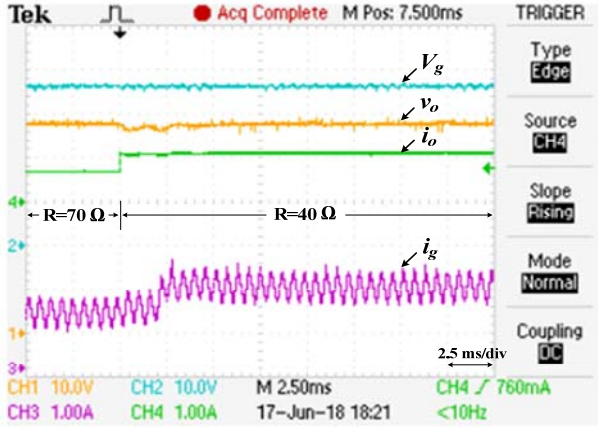
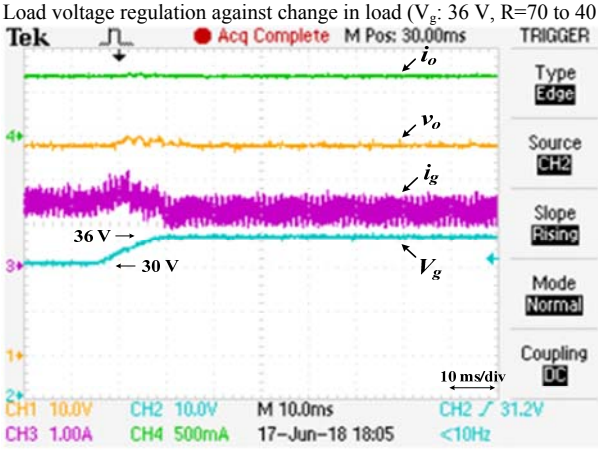


Fig. 11. Steady-state waveforms of SBBC under boost mode of operation (V_g: 36 V, R: 70 Ω).



(a) Load voltage regulation against change in load (V_g: 36 V, R=70 to 40 Ω)



(b) Load voltage regulation against change in source voltage (V_g: 30 to 36 V, R=70 Ω)

Fig. 12. Dynamic performance of SBBC against line and load variations (boost mode of operation).

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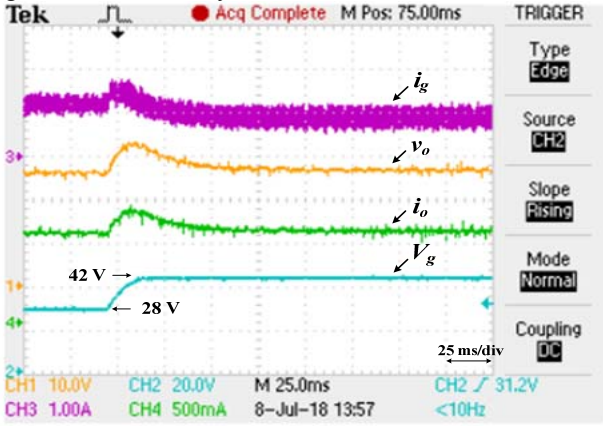
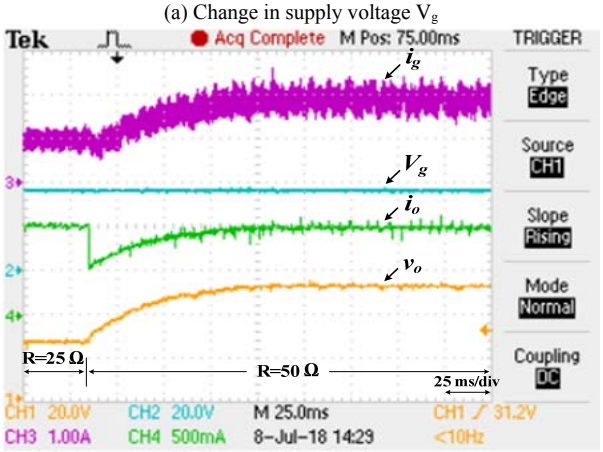
V. CONCLUSION

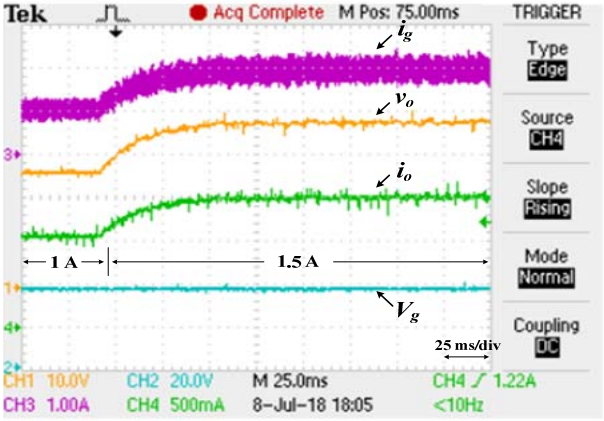
A switching-capacitor based buck-boost converter exhibiting identical voltage gain as that of conventional Buck-boost/Two-switch buck-boost converter was proposed. Detailed analysis revealed that the proposed converter uses the degree of freedom offered by the PWM gating scheme and is able to operate in three different modes (Type-A: buck-boost, Type-B: buck, and Type-C: boost) with minimal structural modifications. Detailed analysis was established and a single-loop controller, voltage-mode/current-mode controller, was designed. The effectiveness of SBBC in closed-loop operation was demonstrated experimentally both for bucking as well as boosting operations. It exhibited low source current ripple content irrespective of its mode of operation (buck-boost, buck, and boost). Furthermore, Type-A operation exhibited seamless transition from buck to boost mode and vice-versa successfully. The measured results are congruent with the analytical studies.



(a) Change in supply voltage V_g



(b) Change in load R



(c) Change in current reference (I_0=1.0 to 1.5 A)

Fig. 13. Dynamic performance of SBBC with current control.

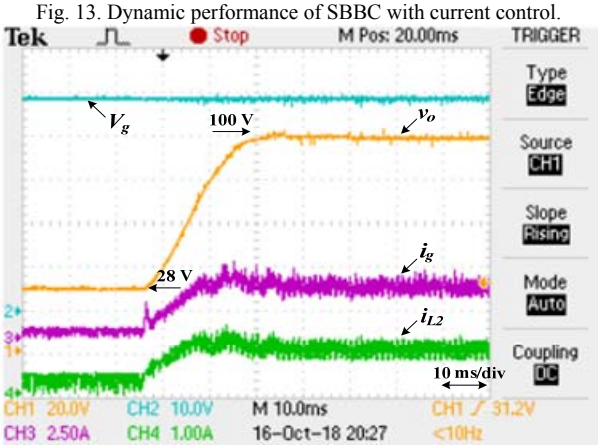


Fig. 14. Dynamic performance of SBBC at higher power level (V_g: 48 V, R: 100 Ω, $V_{0\text{-ref}}$: 28 to 100 V).

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TABLE II-A. COMPARISON OF OTHER BUCK-BOOST TOPOLOGIES WITH PROPOSED CONVERTER

Converter Feature	CBBC [1]	BBIF [4]	CUK [2]	TSBB [6]	TSBBF [16]	BUBS [6]	KYBB [19]	Proposed converter
Switches	1	1	1	2	4	2	2	2
Diodes	1	1	1	2	0	2	1	2
Energy storage elements	2	4	2	2	2	4	5	4
Voltage gain	$\frac{-D}{(1-D)}$	$\frac{-D}{(1-D)}$	$\frac{-D}{(1-D)}$	$\frac{D}{(1-D)}$	$\frac{D}{(1-D)}$	$\frac{D}{(1-D)}$	$2D$	$\frac{D}{(1-D)}$
RHP Zero	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Common ground	NO	NO	NO	YES	YES	YES	YES	YES
Nature of source current	DISC.	CONT.	CONT.	DISC.	DISC.	DISC.	DISC.	CONT.
Ripple in source current	k_{20}	$\frac{k_{21}DT_s}{L_1}$	k_{20}	$\left[k_{23}+\frac{k_{20}}{2}\right]$	$\frac{-k_{22}DT_s}{L_1}$	$(1-D)k_{20}$	$(2I_o+k_{24})$	k_{25}
Multi-mode operation	NO	NO	NO	Yes	Yes	Yes	NO	Yes

$k_{15}=\left(r_2+k_{11}\right)$, $k_{20}=\left(V_gDT_s/L_1\right)$, $k_{21}=[r_{c1}i_2-(r_1+r_{c1})i_1]$, $k_{22}=\left(r_1i_1+r_{c1}i_{c1}\right)$, $k_{23}=I_0/\left(1-D\right)$,
$k_{24}=k_{20}\left(1-D\right)\left(L_1+L_2\right)/2L_2$, $k_{25}=k_{20}\left(2L_1+L_2\right)/L_2$, $D'=(1\text{-}D)$; CONT: Continuous; DISC: Discontinuous

TABLE II-B. COMPARISON OF BUCK-BOOST TOPOLOGIES UNDER MULTI-MODE OPERATION

Parameter		TSBB [6]			TSBBF [16]			BUBS[6]			Proposed converter		
		Buck	Boost	Bubo	Buck	Boost	Bubo	Buck	Boost	Bubo	Buck	Boost	Bubo
No. of devices		3	3	4	3	3	4	3	3	4	3	3	4
Source current profile		Pulsg	Smtw	Pulsg	Smtw	Smtw	Smtw	Pulsg	Smtw	Pulsg	Smtw	Smtw	Smtw
Load side capacitor ripples		$\frac{k_{31}}{L}$	k_{32}	k_{32}	$\frac{k_{31}}{L_2}$	k_{32}	k_{32}	$\frac{k_{31}}{L_2}$	k_{32}	k_{32}	$\frac{k_{31}}{L_2}$	$\frac{k_{31}}{L_2}$	$\frac{k_{31}}{L_2}$
Source ripple		High	Low	High	Low	Low	Low	High	Low	High	Low	Low	Low
Switch Volt. stress	S_1	V_g	0	V_g	V_g	0	V_g	V_g	0	V_g	V_{c1}	V_{c1}	V_{c1}
	S_2	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_0	V_{c1}	0	V_{c1}

Bubo: Buck-Boost; Pulsg: Pulsating; Smtw: Smooth waveform; $k_{31}=v_0D'/f_s$; $k_{32}=\left(\left(I_0/D'\right)+\left(k_{31}/2L_2\right)\right)$